Amendments to the Claims

1. (*Currently Amended*) A process of forming a semiconductor device, comprising:

forming at least one device layer over a wafer surface;

providing a mask over a portion of the device layer; and

using a plasma-etch using first and second etching chemistries, and selectively etching into the device layer to form a pillar structure having at least one sidewall, the selective etching including use of nitrogen in an amount less than about ten percent, of gas flow in a second etching chemistry, as part of the plasma etch in the second chemistry, wherein the amount of nitrogen is maintained to minimize notching in the pillar structure without affecting selectivity.

Claim 2 (*Cancelled*)

3. (*Original*) A process of forming a semiconductor device, according to claim 1, wherein the second chemistry includes nitrogen in an amount less than about two percent of gas flow in the second chemistry.

4. (*Previously Amended*) A process of forming a semiconductor device, according to claim 1, wherein the second chemistry includes a diluted gas mixture of nitrogen.

5. (*Original*) A process of forming a semiconductor device, according to claim 1, wherein the device layer is polysilicon, and the second chemistry includes in an amount less than about ten percent of gas flow in the second chemistry.

6. (*Original*) A process of forming a semiconductor device, according to claim 5, wherein the mask is a hardmask, and the first chemistry includes one of HBr/ Cl_2, HBr/HCl, or HBr/ Cl_2/ Cl_4.

7. (*Currently Amended*) A process, according to claim 6, wherein the first chemistry further includes a selectivity booster.

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8. (*Currently Amended*) A process of forming a semiconductor device, comprising:

forming at least one device layer over an underlying dielectric layer, the device layer and the underlying dielectric layer being over a wafer surface;

providing a mask over a portion of the device layer;

a step of using a plasma-etch of a first chemistry and selectively etching into the device layer for a function of forming a pillar structure having at least one sidewall; and

after the step of using the first chemistry, using a step of using a plasma-etch of a different second chemistry that includes less than about ten percent nitrogen of gas flow in the second chemistry for a function of completing the selective etching upon etching up to the underlying dielectric layer, wherein the amount of nitrogen is maintained to minimize notching in the pillar structure without affecting selectivity.

9. (*Original*) A process, according to claim 8, wherein the device layer includes at least one of: a layer of polysilicon; and an anti-reflective coating on a layer of polysilicon.

10. (*Original*) A process, according to claim 8, wherein the device layer is polysilicon and the pillar structure is a gate electrode.

11. (*Original*) A process, according to claim 10, wherein the mask is a hardmask.

12. (*Original*) A process, according to claim 11, wherein the mask is formed using SiON.

13. (*Original*) A process, according to claim 12, wherein the first chemistry includes HBr/Cl_2. and a selectivity booster.

14. (*Original*) A process, according to claim 12, wherein the first chemistry includes at least one of HBr/Cl_2 and $HBr/ Cl_2/ Cl_4$

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15. (*Original*) A process, according to claim 14, wherein the second chemistry includes nitrogen in an amount less than about ten percent of gas flow in the second chemistry, and wherein the second chemistry includes a diluted gas mixture of nitrogen.

16. (*Original*) A process, according to claim 8, wherein the second chemistry includes nitrogen in an amount less than about two percent of gas flow in the second chemistry.

17. (*Original*) A process, according to claim 8, wherein the second chemistry includes nitrogen in an amount less than about ten percent of gas flow in the second chemistry.

18. (*Currently Amended*) A process of forming a semiconductor device, comprising:

forming at least one gate electrode layer over a gate oxide, the gate oxide being above a wafer surface;

providing a hardmask over a portion of the device layer;

using a plasma-etch of a first chemistry that includes HBr and selectively etching into the device layer to form a pillar structure having at least one sidewall;

after using the first chemistry, using a plasma-etch of a different second chemistry that includes HBr and nitrogen and selectively etching into the device layer to form a pillar structure having at least one sidewall, the second chemistry including nitrogen in an amount less than about ten percent of gas flow of the second chemistry, wherein the amount of nitrogen is maintained to minimize notching in the pillar structure without affecting selectivity; and

terminating the use of a plasma-etch of the second chemistry in response to reaching the gate oxide.

19. (*Original*) A process, according to claim 18, wherein the first chemistry includes one of HBr/ Cl_2, HBr/HCl, or HBr/ Cl_2/ Cl_4, and also includes a selectivity booster.

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20. (*Original*) A process, according to claim 18, wherein the first chemistry includes HBr/ Cl_2 and He-O_2.

21. (*Original*) A process, according to claim 18, wherein the second chemistry includes a diluted gas mixture of nitrogen.

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